Atty. Docket No.: 42390.P2319RC

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
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Marisetty	)	Examiner: To be assigned
	)	
Application No.: To be assigned	)	Art Unit: To be assigned
	)	
Filed: Herewith	)	
	)	
For: (As Amended) Method And Apparatus For Adjusting A Power Consumption Level Based On The Amount Of Time A Processor Clock Is Stopped	)	
	)	
(Previous Title) Method and Apparatus for Reducing Power Consumption in a Computer System Using Virtual Device Drivers	)	
Continuation of:	)	
	)	
Application No.: 09/224,620	)	
	)	
Filed: December 31, 1998	)	
Reissue of US Patent 5,590,342	)	
	)	

Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT
Under 37 CFR § 1.53(b)

Dear Sir:

Applicant respectfully requests entry of the preliminary amendment submitted herewith in the above-referenced patent and consideration of the following remarks. Furthermore, applicant requests priority of the earlier filing date, December 31, 1998, of Application No.: 09/224,620.

Applicant respectfully hereby declares that the ownership of the above referenced reissue application has not changed since filing the reissue application. Furthermore, Intel Corporation

remains the assignee of U.S. Patent No. 5,590,342, as established by the assignment to Intel Corporation recorded at the Patent Office at reel 7341, frames 0694 and 0695 on January 24, 1995.

IN THE TITLE

Please change the title to "Method And Apparatus For Adjusting A Power Consumption Level Based On The Amount Of Time A Processor Clock Is Stopped".

IN THE SPECIFICATION

Please insert as the first sentence of the specification, "This is a continuation of application Serial No. 09/224,620 filed on December 31, 1998."

IN THE CLAIMS

Please cancel claims 1-35.

Please cancel claims 36-50 (to the extent they would be present in this application).

Please add the following Claims.

51. A machine-readable medium having stored thereon instructions, which if executed by a machine, cause said machine to perform operations comprising:

determining an amount of time a processor is in a first power consumption state, said amount of time said processor is in said first power consumption state comprising a period of time in which a clock of said processor is stopped;

reducing a voltage level applied to said processor in response to said

amount of time said processor is in said first power consumption state.

52. The machine-readable medium of Claim 51 wherein reducing said voltage level applied to said processor is performed in response to said amount of time exceeding a selected amount of time.

53. The machine-readable medium of Claim 52 wherein determining comprises reading a timer to determine said amount of time said processor is in said first power consumption state.

54. The machine-readable medium of Claim 53 wherein said reducing said voltage level comprises placing said processor in a power-off state.

55. The machine-readable medium of Claim 51 wherein determining the amount of time said processor is in the first power consumption state comprises monitoring an activity level demand within a computer system.

56. The machine-readable medium of Claim 55 wherein reducing the voltage level applied to the processor comprises operating said processor in a reduced power consumption state while satisfying said activity level demand.

57. A machine-readable medium having stored thereon instructions, which if executed by a machine, cause said machine to perform operations comprising:

determining an amount of time a clock of a processor is stopped;

placing said processor into a reduced power consumption state in response to said amount of time said clock of said processor is stopped.

58. The machine-readable medium of Claim 57 wherein said placing comprises reducing a voltage of said processor.

59. The machine-readable medium of Claim 58 wherein said determining an amount of time said clock of said processor is stopped contributes to determining a system idle time.

60. The machine-readable medium of Claim 59 wherein said clock of said processor is stopped when the processor is in a sleep state.

61. The machine-readable medium of Claim 60 wherein a timer is read to determine said amount of time said processor is in said first power consumption state.

62. The machine-readable medium of Claim 61 wherein said reduced power consumption state is a power-off state.

63. The machine-readable medium of Claim 58 wherein reducing said voltage of said processor is performed in response to said amount of time said clock of said processor is stopped exceeding a selected amount of time.

64. An apparatus comprising:

a power management module to determine an amount of time a processor is in a first power consumption state, said first power consumption state comprising a period in which said processor is stopped;

a power reduction module to place said processor into a reduced power consumption state in response to said amount of time said processor is in said first power consumption state.

65. The apparatus of Claim 64 wherein said power reduction module comprises a software routine.

66. The apparatus of Claim 64 wherein said power management module comprises a timer.

67. The apparatus of Claim 65 wherein said power management module comprises a timer.

68. The apparatus of Claim 67 wherein said power reduction module is enabled to reduce a voltage applied to said processor.

69. The apparatus of Claim 68 wherein said power reduction module is enabled to reduce said voltage in response to said amount of time exceeding a selected amount of time.

70. The apparatus of Claim 69 wherein said power management module comprises a software routine.

71. The apparatus of Claim 70 wherein said first power consumption state is a sleep state.

72. The apparatus of Claim 71 wherein said reduced power consumption state is a power-off state.

73. An apparatus comprising:

a power management module to determine an amount of time a processor is in a first power consumption state, said first power consumption state comprising a period in which said processor is stopped;

a power reduction module to place said processor into a reduced power

consumption state in response to said amount of time said processor is in said first power consumption state, said power reduction module comprising a software routine, said power management module comprising a timer.

74. A system comprising:

a memory;

a processor coupled to said memory;

a power management module to detect an amount of time said processor is in a first power consumption state, said first power consumption state comprising a period of time in which a clock of said processor is stopped, said processor being placed into a reduced power consumption state in response to said amount of time said processor is in said first power consumption state.

75. The system of Claim 74 wherein said reduced power consumption state comprises a reduced voltage state of said processor.

76. The system of Claim 75 wherein said reduced voltage state comprises a power-off state.

77. The system of Claim 76 wherein said power management module is enabled to determine a system idle time.

78. The system of Claim 77 wherein said system idle time is represented by said amount of time said processor is in said first power consumption state.

79. The system of Claim 78 wherein said first power consumption state is a sleep state.

80. The system of Claim 79 wherein said power management module comprises a software routine.

81. The system of Claim 74 wherein said power management module comprises a software routine.

82. The system of Claim 74 wherein said power management module further comprises a timer.

83. The system of Claim 81 wherein said power management module further comprises a timer.

84. The system of Claim 74 further comprising

a configurable device;

power management software to power manage said configurable device.

85. The system of claim 84 further comprising:

power management software to cooperate with said device manager to allow power management of a plurality of devices in the system which are configurable devices, and to manage a power level for each of the plurality of devices in the system. the power management software being capable of placing one or more of said plurality of devices in a reduced power consumption state.

86. The system of claim 85 further comprising a plug and play manager.

87. The system of claim 86 wherein said power management software is to communicate with said plug and play manager to update data structures if configuration changes occur to allow power management of dynamically reconfigurable devices.

88. The system of claim 87 wherein said power management software registers with said device manager to be notified of configuration changes.

89. The system of claim 88 wherein said power management software is to provide

system level power management including the use of multiple system level power management states for said system, and to provide multiple power management states for said plurality of devices.

90. The system of claim 88 wherein said power management software is to provide support for idle detection for at least one of said plurality of devices.

91. The system of claim 88 wherein said power management software is to place the system in a sleep state when the system is idle and to keep said system in said sleep state until activity is detected, and wherein the sleep state is one of a plurality of system power management states, and further wherein said system stops a clock for a system processor in said sleep state.

92. A method comprising:

determining an amount of time a clock of a processor is stopped;

placing said processor into a reduced power consumption state in response to said amount of time said clock of said processor is stopped.

93. The method of Claim 92 wherein said placing comprises reducing a voltage of said processor.

94. The method of Claim 93 wherein said determining said amount of time said clock of said processor is stopped contributes to determining a system idle time.

95. The method of Claim 94 wherein said clock of said processor is stopped when the processor is in a sleep state.

96. The method of Claim 95 wherein a timer is read to determine said amount of time said processor is in a first power consumption state.

97. The method of Claim 96 wherein said reduced power consumption state is a power-off state.

98. The method of Claim 97 wherein reducing said voltage of said processor is performed in response to said amount of time said clock of said processor is stopped exceeding a selected amount of time.

99. The method of claim 98 further comprising power managing in cooperation with a device manager a plurality of devices in a system which are configurable devices; and managing a power level for each of the plurality of devices in the system, the power managing comprising placing one or more of said plurality of devices in a reduced power consumption state.

100. The method of claim 99 wherein said system comprises a plug and play manager.

101. The method of claim 100 wherein said power managing comprises communicating with said plug and play manager to update data structures if configuration changes occur to allow power management of dynamically reconfigurable devices.

102. The method of claim 101 further comprising registering power management software with said device manager to be notified of configuration changes.

103. The system of claim 102 wherein said power managing comprises providing system level power management including the use of multiple system level power management states for said system, and to provide multiple power management states for said plurality of devices.

104. The method of claim 102 wherein said power managing comprises supporting idle detection for at least one of said plurality of devices.

105. The method of claim 102 wherein said power managing comprises placing the

system in a sleep state when the system is idle and to keep said system in said sleep state until activity is detected, and wherein the sleep state is one of a plurality of system power management states, and further wherein said system stops a clock for a system processor in said sleep state.

REMARKS

Applicant has numbered the present set of claims starting with claim 51 based on the fact that the parent reissue application was originally filed with a preliminary amendment adding claims up to claim 50. Applicant will gladly renumber these claims if the chosen numbering is incorrect.

Applicant submits that all claims now pending are in condition for allowance. Such action is earnestly solicited at the earliest possible date. If there is a deficiency in fees, please charge our Deposit Acct. No. 02-2666.

Respectfully submitted,

BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP

Date: 2-21-02

Jeff Draeger
Reg. No.: 41,000

12400 Wilshire
Seventh Floor
Los Angeles CA 90025-1030
(408) 720-8300

"Express Mail" mailing label number: EL 435561785US
Date of Deposit: February 21, 2002
I hereby certify that I am causing this paper or fee to be deposited with the United States Postal Service "Express Mail Post Office to Addressee" service on the date indicated above and that this paper or fee has been addressed to the Assistant Commissioner for Patents, Washington, D. C. 20231

Conny Willesen
(Typed or printed name of person mailing paper or fee)

Conny Willesen
(Signature of person mailing paper or fee)

2-21-02
(Date signed)